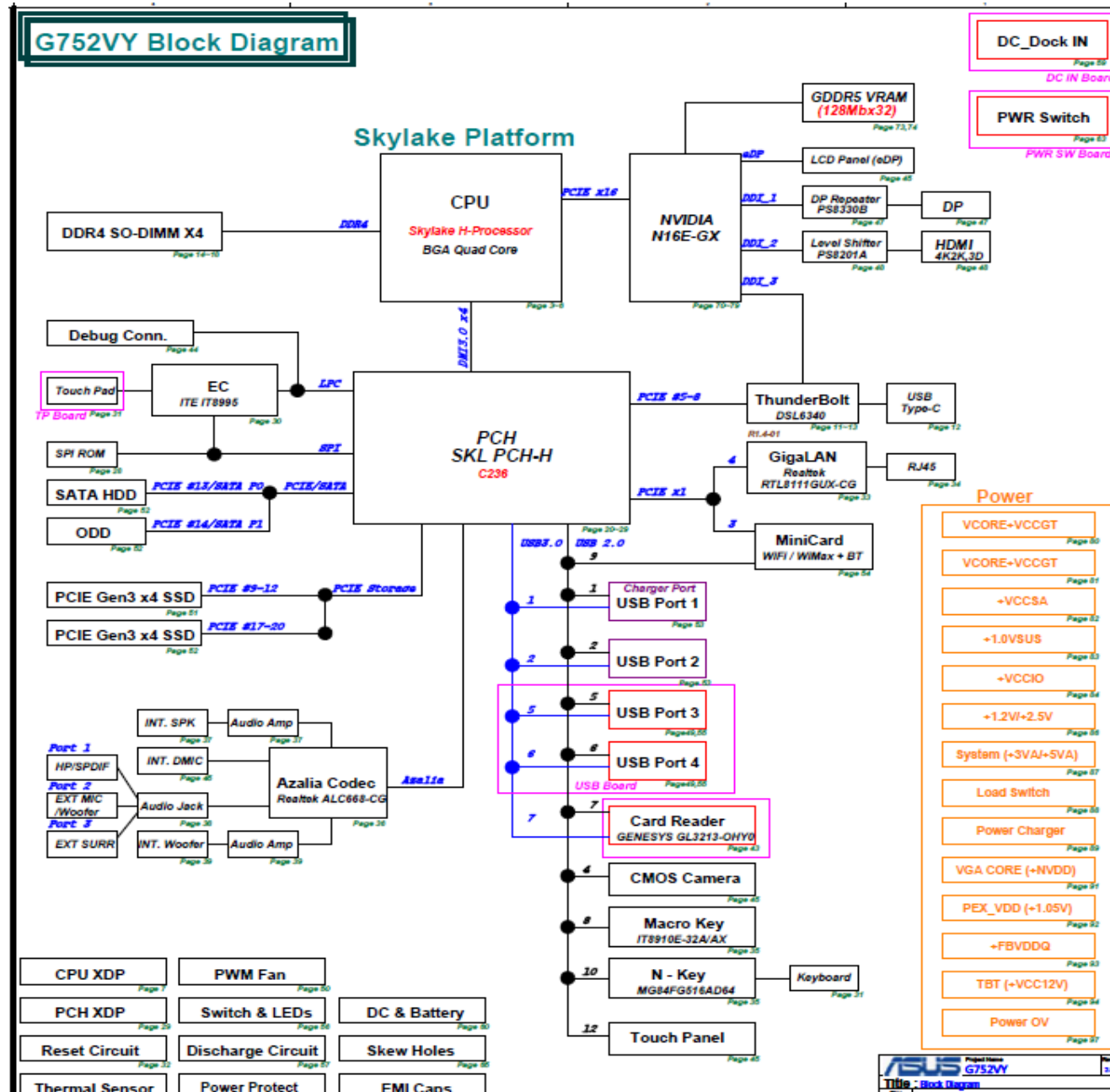
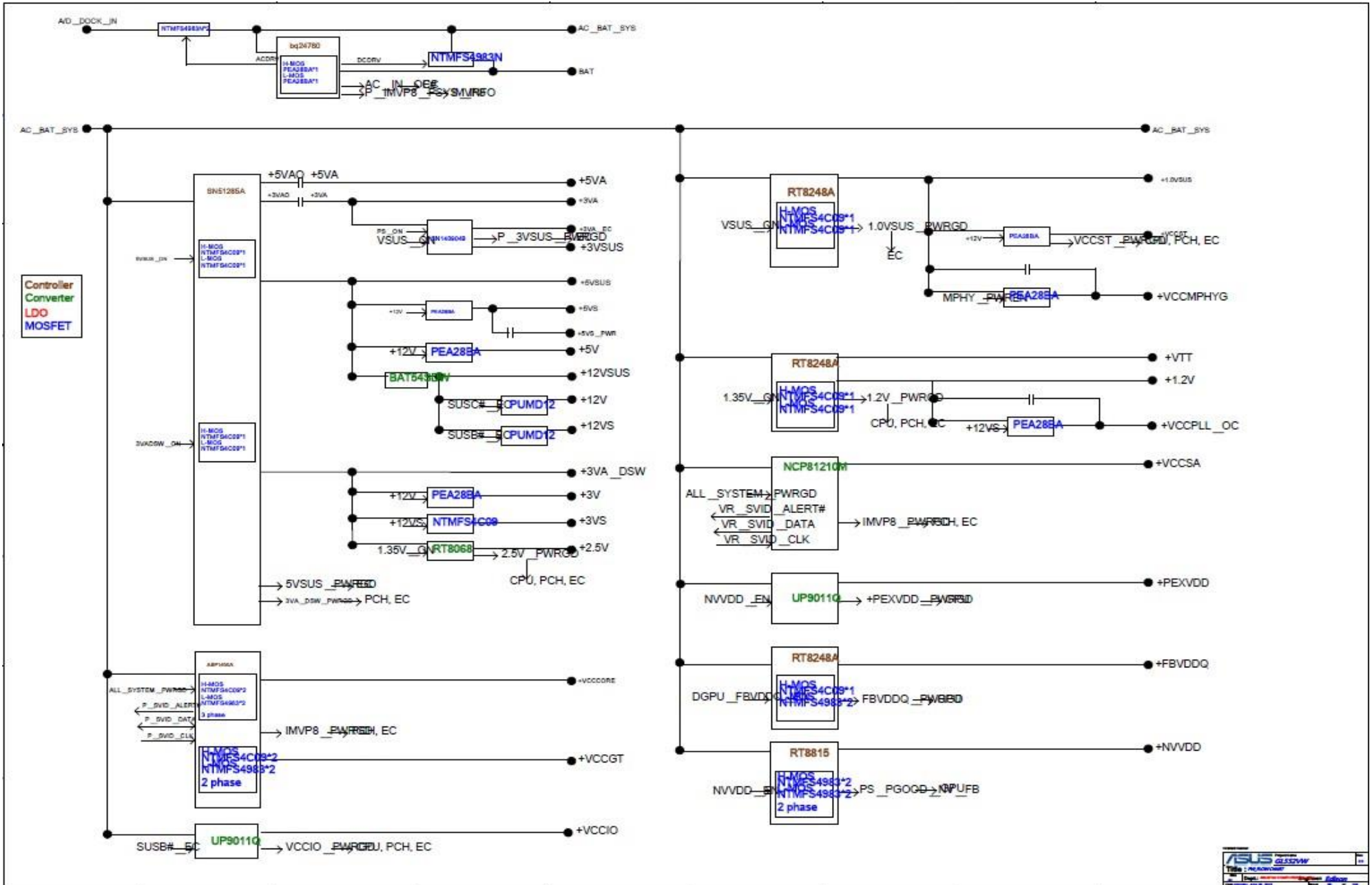


## BLOCK DIAGRAM



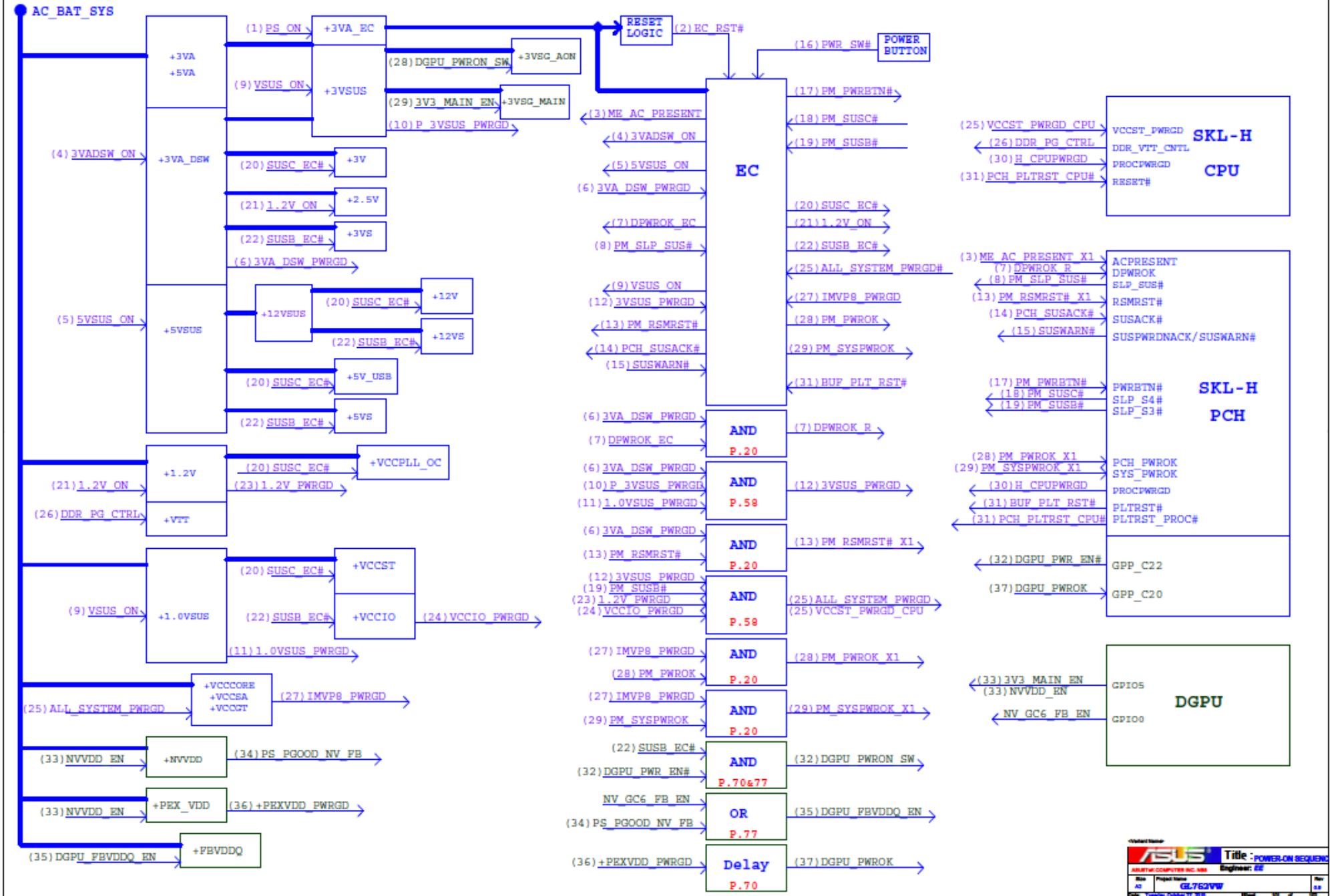
# POWER FLOW



# POWER ON SEQUENCE

AC-IN Mode

GL752VW Power On Sequence Diagram Rev.1.0

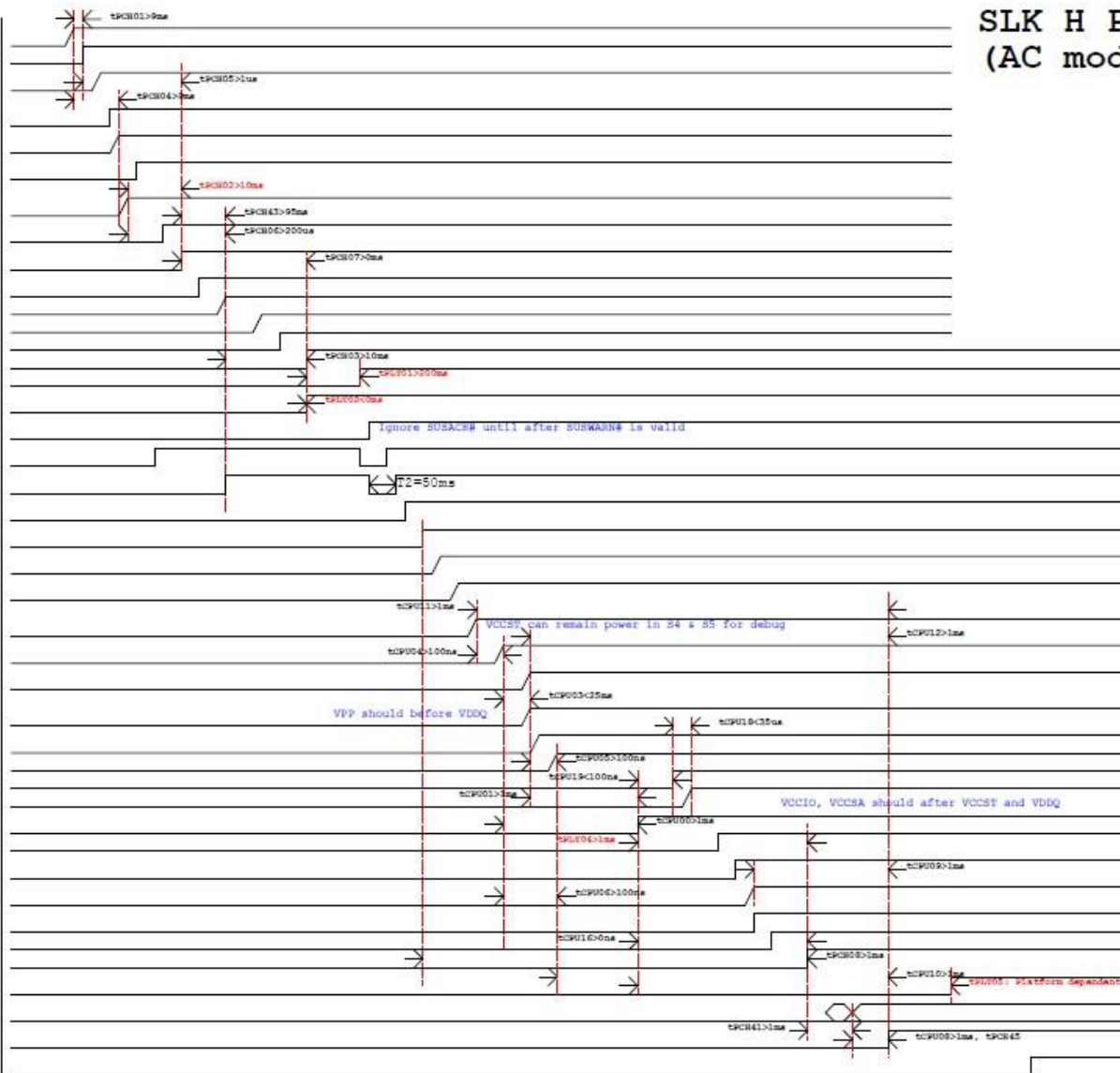


# AC\_IN POWER ON SEQUENCE

## AC-IN Mode

Power  
Signal

(1) +3VA/+5VA  
(2) PS\_ON  
(3) +3VA\_EC  
(4) +EC\_RST#  
(5) +3VA\_DSW  
(6) 3VA\_DSW\_PWRGD  
(7) DPWRK\_EC  
(8) PM\_SLP\_SUS#  
(9) +3VSUS7/+1.0VSUS  
(10) +12VSUS/+5VSUS  
(11) 3VSUS\_PWRGD  
(12) PM\_RSMRST#  
(13) SUSWRN#  
(14) ME\_AC\_PRESENT  
(15) PCH\_SUSACK#  
(16) PWR\_SW#  
(17) PM\_PWRBTN#  
(18) PM\_SUSC#  
(19) PM\_SUSB#  
(20) +12V/+5V/+3V/+VCCST  
(21) +12VS/+5VS/+5VS\_PWR/+3VS/+VCCPLL\_OC  
+1.0V\_VCCST, VCCPLL  
+VCCSTG  
+VCCPLL\_OC  
(22) +1.2V  
(23) +2.5V  
+VCCIO  
DDR\_VTT\_CTRL  
+VTT  
(24) ALL\_SYSTEM\_PWRGD  
(25) P\_IMVP8\_EN\_10  
(26) P\_IMVP8\_DRVON  
+VCCCORE/+VCCGT/+VCCSA  
(27) IMVP8\_PWRGD  
(28) VCCST\_PWRGD\_CPU  
(29) PM\_PWRK  
(30) PM\_SYSPWRK  
CLK\_PCH\_BCLK  
(31) H\_CPU\_PWRGD  
(32) PCH\_PLTRST\_CPU#

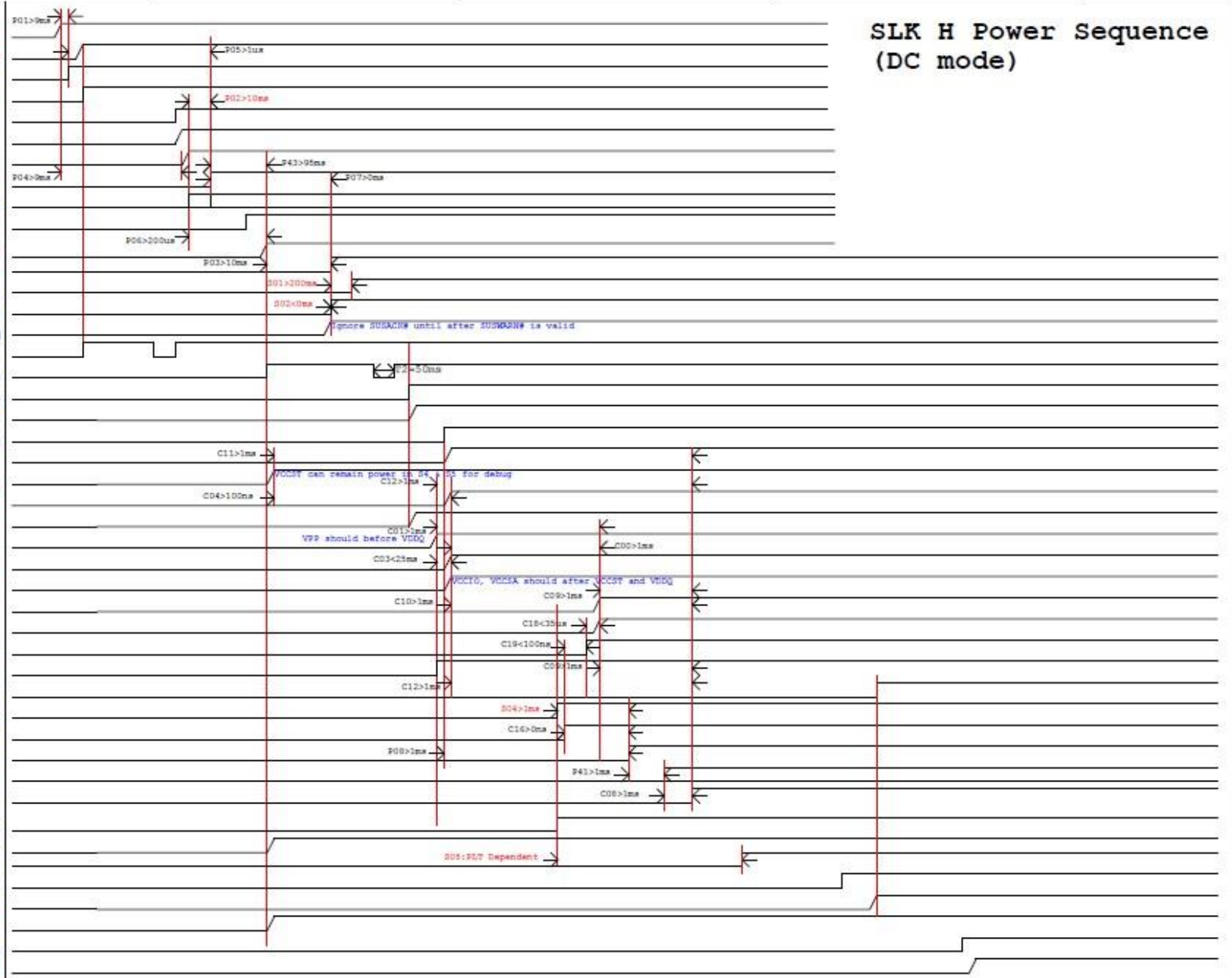


## SLK H Power Sequence (AC mode)

# DC\_IN POWER ON SEQUENCE

## DC-IN Mode

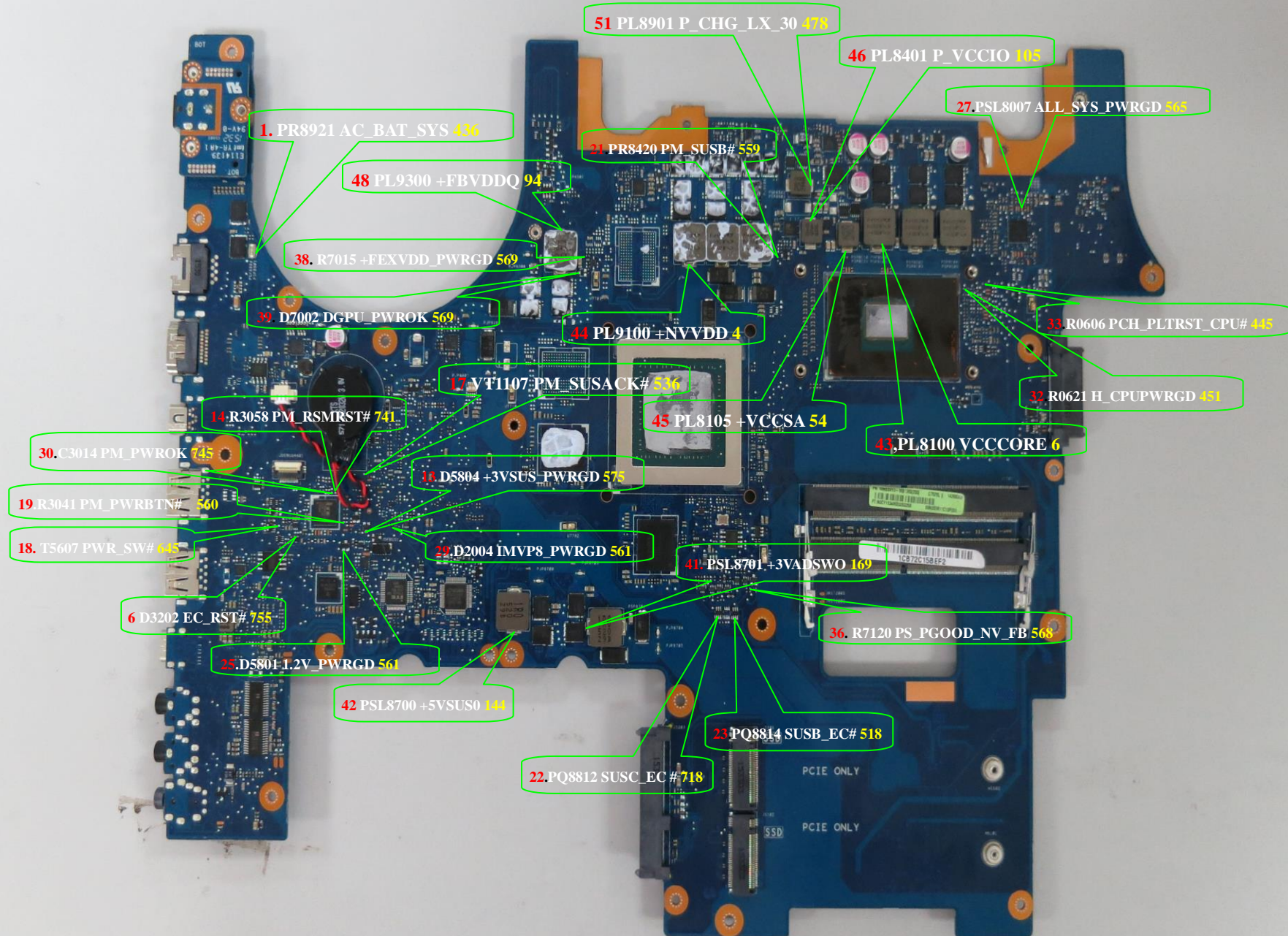
C:CPU (+RTCBAT)+3VA\_RTC  
 P:PCH (AC\_BAT\_SYS)+3VA/+5VA  
 S:PLT (+3VA\_RTC)RTCRST#(PCH)  
 Power (Power)AC\_IN\_OC#(EC)  
 Signal (EC)PS\_ON(+3VA\_EC)  
 (PS\_ON)+3VA\_EC(EC)  
 (3VADSW\_ON)+3VA\_DSW(3VA\_DSW\_PWRGD)  
 (EC)DPWRON\_EC(PCH)  
 (+3VA\_DSW)PM\_BATLOW#(PCH)  
 (PCH)PM\_SLP\_SUS#(EC)  
 (VSUS\_ON)+1.0VSUS\_VCCPRIM(1.0VSUS\_PWRGD)  
 (EC)PM\_RSMRST#\_PCH(PCH)  
 (PCH)SUSWAKE#(EC)  
 (EC)ME\_AC\_PRESENT\_PCH(PCH)  
 (EC)PCH\_SUSACK#(PCH)  
 (PWR\_Switch)PWR\_SW#(EC)  
 (EC)PM\_PWRBTN#(PCH)  
 (EC)SUSC\_EC#(Power)  
 (SUSC\_EC#)+12V/+5V/+3V  
 (EC)SUSB\_EC#(Power)  
 (SUSB\_EC#)+12VS/+5VS/+3VS  
 (VSUS\_ON)+1.0V\_VCCST,VCCPLL(VCCST\_PWRGD)  
 (+VCCIO)+VCCSTG  
 (1.2V\_ON)+2.5V(2.5V\_PWRGD)  
 (1.2V\_ON)+VDDQ\_CPU(1.2V\_PWRGD)  
 (+12VS)+VCCPLL\_OC  
 (SUSB\_EC#)+VCCIO(VCCIO\_PWRGD)  
 (ALL\_SYSTEM\_PWRGD)+VCCSA(IMVP8\_PWRGD)  
 (DDR\_VTT\_CTRL)+0.6V  
 (CPU)DDR\_VTT\_CTRL(Power)  
 (Power)1.2V\_PWRGD(AND)  
 (Power)IMVP8\_PWRGD  
 (AND)ALL\_SYSTEM\_PWRGD(CPU/PCH/EC/Power)  
 (ALL\_SYSTEM\_PWRGD)VCCST\_PWRGD\_CPU(CPU)  
 (EC)PM\_PWRON\_PCH(PCH)  
 (PCH)CLK\_PCH\_BCLK(CPU)  
 (PCH)H\_CPUPWRGD(CPU)  
 (ALL\_SYSTEM\_PWRGD)P\_IMVP8\_EN\_10(Power)  
 (CPU)P\_SVID\_DATA\_X2(Power)  
 (EC)PM\_SYSFWROK\_PCH(PCH)  
 (PCH)PLT\_RST#(CPU/EC/Device)  
 (P\_IMVP8\_DRVON)+VCCCORE(IMVP8\_PWRGD)  
 (CPU)H\_THERMTRIP#(PCH)  
 (PCH)DDR4\_DRAMRST#(Memory)  
 +VCCGT



## SLK H Power Sequence (DC mode)



## Signal Measure Point-Bottom





# Signal Measure Point-Top

